# Lab 3 Structural Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? \_yes\_\_

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here. Otherwise write “n/a”: **\_\_n/a\_\_**

Student Name: Chris Cyr  
Student ID: 12436037  
Date Completed: 5/28/2022  
Time Spent: Reviewing Digital Design Material: 8hrs  
 Design/Preparation Work: 2hrs  
 VHDL Coding & Debugging: 4hrs

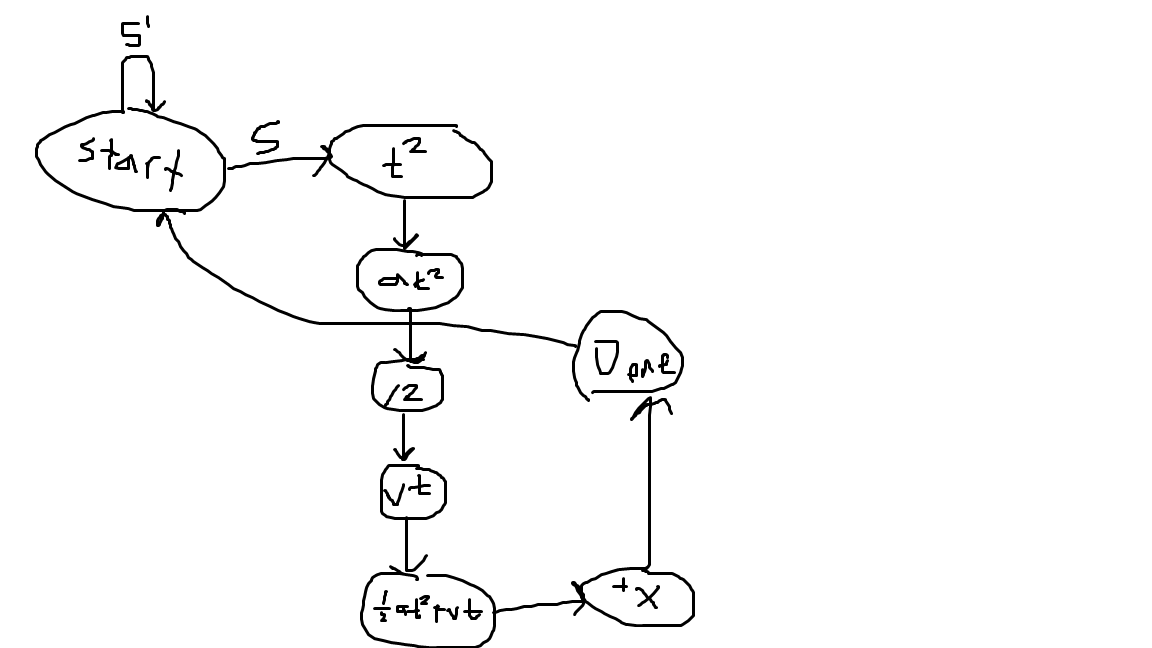
## Structural Overview

What % do you feel you completed on the lab? Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

\_\_100%\_\_

## Lab 3 FSMD & Control Word Table

Show your final FSMD here (even if nothing’s changed). Explain why anything has changed or hasn’t changed.



All of the states reset when reset is 1 but I didn’t draw that for clarity

Show your control word table for your design here.



## Lab 3 Minimum Clock Cycle

Minimum clock cycle: 37ns

Explain how you derived your minimum clock cycle (as discussed in class) here.

## Lab 3 Structural Simulation Graph

Show a screenshot or multiple screenshots of your final graph here. You should crop it to the appropriate size so that it is legible. All relevant test case information and signals should be shown.

A screenshot of a computer

Description automatically generated with medium confidence

## Lab 3 Structural and Behavioral Simulation Graph Comparisons

Compare your behavioral & structural graphs here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence